Design Technique of Phase-Locked Loop Frequency Synthesizer in CMOS Technology: A Review

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Abstract—**This paper deals with different approaches to design Phase Locked Loop (PLL) frequency synthesizer. PLL system responds to both frequency and phase of the input signals, automatically raising or lowering the frequency of controlled oscillator until it is matched to the reference in both frequency and phase. The performance of PLL frequency synthesizer is improved by using different Voltage controlled Oscillator (VCO) and their varactor or magnetic tuning scheme. It is generally desired to design low phase noise, wide tuning, low power consumption, high quality factor and independent to Process, Voltage, and Temperature (PVT) variation. Today's CMOS IC technology is used in many critical design aspects such as thermal noise cancelling, low-frequency noise reduction on MOSFETs, and distortion cancelling. However, here various improvements in technology from µm to nm, supply voltage from 0.7 to 1.8V, frequency generated from 2 to 78 GHz and tuning range from 10 to 23% are discussed.**

Keywords— **Frequency Synthesizer (FS), Phase Locked Loop (PLL), Voltage Controlled Oscillator (VCO), Low Noise Amplifier (LNA), Process, Voltage, and Temperature (PVT), Frequency Modulated Continuous Wave (FMCW).**

I. INTRODUCTION

A frequency synthesizer (FS) is a feedback system that generates one or many frequencies from one or a few frequency sources. The output of an FS is characterized by its frequency tuning range, frequency resolution, and frequency purity but some uncertainty of a synthesizer's output is characterized by its phase noise (or spur level) at a certain frequency offset from the desired carrier frequency in unit of dBc/Hz (or dBc*)*. The unit of dBc/Hz measures the ratio (in dB*)* of the phase noise power in 1Hz bandwidth at a certain frequency offset to the carrier power. Frequency synthesizers can be grouped into two classes: direct synthesis and indirect synthesis. Direct synthesis is classified in direct analog synthesizer (DAS) and direct digital synthesizer (DDS). Indirect synthesis is classified in phase-locked loop frequency synthesizer (PLL-FS), and delay-locked loop frequency synthesizer (DLL-FS). In this paper focused on PLL based frequency synthesizer. It is categories in integer-*N* and fractional-*N* synthesizer on the basis of programmable divider. Phase-locked loop is control system which produce a replica of an input frequency or the signal generated by PLL have a fixed relation with the phase/frequency of the input signal. Phase-locked loop is a closed loop control system that compares the output phase with the input phase. It responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. It is an example of a control system using negative feedback which tracks the phase changes that are within the bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock to produce a high-frequency clock. The phase-locking is done after many iterations of comparing the reference and feedback signals. As the phase is locked then the output of PLL will be constant. Phase-locked loop consist of phase/frequency detector, charge pump, low pass filter, voltage controlled oscillator and programmable divider. The phase-frequency detector detects any phase differences between the input reference signal and the feedback signal generate digital error pulse that digital error pulse converted in to analog error current by charge pump that provided to low pass filter which integrates error current to generate control voltage supplied to VCO which converts that control voltage in to signal with appropriate frequency. As the control voltage is increase than VCO signal frequency also increase. The output signal from VCO is divided by a programmable divider and compared with input signal in phase frequency detector and generate error pulse. This process is continue until the phase difference between the input reference signal and the feedback VCO signal is zero or constant that is the locked state. This process is called phase tracking. The time PLL takes to respond to change in the input frequency is called as lock time and the range of frequency over which the PLL can stay in lock is called the hold in range. Ideally, the lock time should be small as possible. It plays an important role in wide range of applications including clock de-skew for high-speed digital and mixed-signal IC's, clocks synthesis, carrier recovery, clock recovery, modulation and demodulation of frequency or phase and filter tuning [8].

At present time 65 or less nanometer CMOS scale is quite popular in research for PLL. A dual gate device for *Ka-* band broadband LNA and high accuracy quadrature voltage controlled oscillator was used to generate 19 to 27GHz frequency. This duel gate CMOS design result was independent of PVT variation for linear and nonlinear circuit designs above 20GHz especially for high speed system.

For wide tuning range a resonant mode switching was presented in 2012 by Guansheng Li, It was operated at 0.6

V power supply and covered 2.5 to 5.6GHz cellular bands with excellent phase noise.

At near in future for radar application, digitally-controlled oscillator would be used in transmitter.

From resent research in 2014, a 56.4 to 63.4GHz multi-rate All-Digital Fractional-*N* PLL for FMCW Radar Applications in 65-nm CMOS process has presented. It introduced a design to achieve high gain and more stability in system by using transformer-coupled to the 3-stage Power amplifier (PA) at synthesizer output. It delivers 5dBm into a 50- load and consumes 89mW from a single 1.2-V supply.

In this paper, focus on 0.7 - 1.8V CMOS PLL- FS with a wide tuning range and low sensitivity to PVT variations is presented in the µm - nm technology. It also includes extensive overview to design of robust PLL and improve its performance. In the following sections initially PLL-FS system is discussed. It is followed by modification of PLL design with the conclusion based on review.

II. PLL-FS SYSTEM

Frequency generator is at the heart of every transmitter and receiver. Digital control and phase-locked loop frequency synthesis are such a perfect fit it is hard to imagine any modern frequency agile/fast oscillator without phase lock control.

Analog frequency demodulation uses the basic PLL. Their demodulated signal is actually the VCO control voltage. In frequency demodulation the PLL loop bandwidth is wide, so that the VCO output frequency tracks the input frequency but in phase demodulation PLL loop bandwidth is narrow, so that the output frequency tracks the input carrier frequency and output phase is the average of input phase. The PLL output frequency can be either an integer or fractional times of reference frequency by virtue of which frequency locking in PLL used the integer-*N* or fractional-*N* divider. Digital PLL generates a clock signal in synchronization with the incoming signal. Receiver circuits use this clock signal to provide clock to the shift register to recover the data. This application of digital PLL is often termed a clock recovery circuit or bit synchronization circuit. The clock and data recovery based PLL is to synchronize the random data to a clock signal generated by VCO in the PLL [11].

In design of direct analog synthesizer (DAS) is realized by cascading stages of frequency multipliers, dividers, mixers and band-pass filters (BPF). It generates large number of separate frequencies from a single reference and rapidly switched between any set of frequency. Many manufactures used this design and they report that excellent phase noise and spurious performance at desired frequency but its sheer size and power consumption make this synthesizer to limited application in1960's. To improve the signal band and reduce power consumption direct digital synthesizer was presented in early 1970's. It has two major components numerically controlled oscillator (NCO) and a digital to analog converter (DAC). NCO consists of an adder-register pair (phase accumulator) and a ramp to sine wave lookup ROM. It provides a low frequency output with extremely high resolution and excellent frequency

switching speed. But due to sampling theory DDS can only generate frequency up to maximum of half of the clock rate of the digital circuit and it has also high spurious content caused by quantization and linearity limitation of the DAC. Here a rough rule of thumb is that the spurious level generated by DAC quantization equals 6dB times the number of input bits [4].

For large frequency DDS can't be efficient due limitation of DAC. In 1990's integer-*N* and fractional-*N* PLL frequency synthesizer is introduced. It generates frequency in GHz with robust system. Integer-*N* PLL consists of phase-frequency detector (PFD), a charge pump (CP), a loop filter, a voltage controlled oscillator (VCO), and a programmable frequency divider. Its output frequency is integral multiple or loop frequency divider ratio of reference frequency. The frequency resolution of this synthesizer is equal to reference frequency. It causes large lock time. Their reference spur and its harmonic will be located at low offset frequency. For large frequency, divider ratio also large and causes in-band phase noise associated with the reference signal. So with low loop band width, phase noise at low off set frequencies can't sufficiently suppress. It required a large loop band width.

To increase the loop band width with same reference frequency Fractional-*N* PLL frequency synthesizer is used, it also overcome the defect and full fill deficiency of Fractional-*N* PLL synthesizer. Here frequency divider can be fractional and a large reference can be used to achieve a small frequency resolution. However to design the fractional divider dual –modulus or multi modulus technique is used which have a fixed pattern and it cause unwanted low-frequency spur. Practically fractional-*N* synthesizer can't suppress in-band spur at negligible level but in literature five main spur reductions techniques are addressed such as DAC phase estimation, Random jittering, ΣΔ noise shaping, phase interpolation and pulse generation [6].

To avoid the large division ratio in an integer-*N* PLL synthesizer, one alternative is to use multiple loops to reduce the division ratio. Dual-loop PLL is frequently used to improve the tradeoff among phase noise, channel spacing, reference frequency and the locking speed. PLL1 is used to generate reference frequencies for PLL2 and PLL1 output is up-converted by PLL2 and a single-sideband (SSB) mixer. PLL1 generates tunable IF frequencies, while PLL2 generates a fixed RF frequency. Mixer is used to reduce the divide ratio in PLL1. Recent works used the dual-loop PLL topology for GSM receivers. The drawback of the dual-loop PLL is that it may require two references, and at least one SSB mixer, which might introduce additional phase noise. For overcome the effect of phase noise in system Delay Lock Loop frequency synthesizer is introduced. It has no phase accumulation and extremely low phase noise can be achieved but the big drawback of the DLL frequency synthesizer is that it is not programmable. Other problems, such as limited multiplication factor and high power consumption also limit its application.

At present time a mixed signal frequency synthesizer is more popular and many systems incorporate a mixture or hybrid of these basic approaches in order to take advantage

of the benefits of increased speed or improved resolution that one approach may have over another. Sometimes a PLL synthesizer may incorporate a DDS in its reference circuitry to increase resolution or to reduce switching time. A major drawback of this approach is that the PLL acts as a multiplier on any phase noise or spurs and a DDS may have high spurs. The resulting noise at PLL output can seriously degrade system performance [3].

III. MODIFICATION IN PLL DESIGN

Today is the world of electronics and the size of their products are regularly decreasing but its efficiency and reliability increasing due to explosive growth in VLSI technology. Wireless communication has led to increased demand for products that are low cost, low power, and compact in size. Recently CMOS technology is used to design RF components such as low-noise amplifiers, mixers and VCO because it easily achieve high level of RF/analog/ digital integration in single chip system implementations. VCO is a key component of PLL-FS for RF wireless applications, so a large number of research papers are published on improvement of VCO and other essential components of PLL-FS.

Bunch *et al.* has carried many experiment on large signal effect in different MOS varactors and simulated result compared with a design of 2.5 GHz complementary –Gm LC VCO using I-MOS varactors implemented in 0.35-μm CMOS technology. In this analysis focus on large signal swing of VCO output depends on different varactor capacitance such as D=S=B, A-MOS, and I-MOS structure. Here A-MOS and I-MOS structure shown linear tuning scheme which is essential for PLL application. It used a standard approach for differential VCO and generates negative resistance by cross-coupled transistors pair for desired oscillation. It is operated at 3.3 V supply and its phase noise is -103.6 to -123.5dBc/Hz at 100/600 kHz offset. Main motto of this work was to design a VCO with linear tuning gain [7]. For improvement in phase noise use simple routing and minimizes interconnect capacitances, parasitic resistances of interconnects, and provide inherent common-centered characteristic for high frequency VCO.

Young Lee *et al.* proposed cross-coupled transistor structure is applied for a 26.2-GHz differential VCO design which dissipates 7.3mA from 1.8-V supply using 0.18-μm CMOS. The VCO with the proposed transistor structure shows the phase noise of −113.7dBc/Hz at 1 MHz, which corresponds to FOM and FOM_T of −190.4 and −194dBc/Hz, respectively [1]. Its chip size and phase noise performance is improved than Bunch et al. VCO.

Po Wang *et al.* design a circuit topology by applying varactors connected between drain and source terminations of the cross coupled pair, the tuning range is effectively increased and the phase noise is improved. Moreover, a small capacitor is inserted between the VCO core and testing buffer to reduce loading effects on the VCO core. It is operated at 1.2 V and consumes 7.5-mW dc power, and the measured phase noise is −75dBc/Hz and −91.5dBc/Hz at 100 kHz and 1-MHz offsets from the 77.8GHz carrier, respectively. Compared with previously published silicon-based VCOs over 70 GHz, this work can simultaneously

achieve low phase noise, wide tuning range, and low dc power consumption [12].

In order to increase the VCO tuning range, the switched-capacitor resonator and switched-inductor resonator have been proposed [2]. The advantage of both architectures over the varactor tuned single resonator is that the VCO gain is reduced. However, the switch loss can degrade the resonator quality factor and therefore the oscillator phase noise. Although large switches have less loss but, they have larger parasitic capacitance that can degrade the frequency tuning range. Finally, the chip area of a conventional switched-inductor resonator becomes too large due to using several on-chip inductors. In order to reduce the variations of the VCO gain, a pseudo exponential capacitor bank structure, rather than a conventional binary weighted capacitor bank, has been used to implement a wideband VCO [2].

Safarian *et al.* designed an integrated voltage-controlled oscillator (VCO) with a 1.28–6.06 GHz tuning range is designed and fabricated in a 0.13 um CMOS technology. The triple-mode VCO uses a sixth-order resonator based on three coupled inductors with a compact common-centric layout. Depending on the oscillation frequency, the VCO current consumption is automatically adjusted from 2.9 to 6.1mA to achieve a low phase noise throughout the frequency range. The measured phase noises at 1 MHz offset from carrier frequencies of 1.76, 2.26, 3.3, 4.5, and 5.6 GHz are -119.3, -120.15, -118.1, -117, and -113.5dBc/Hz respectively. The chip area, including the pads, is 1 mm 1 mm and the supply voltage is 1.5 V. In this design a 9-bit shift register has been used for transferring the digital bits from the computer to the VCO in a serial manner in coarse tuning and is operated to transfer voltage from 0 to 1.5V in three modes. Mode 1 covers approximately from 1.3 to 2.3 GHz, mode 2 covers from 2.3 to 4.0 GHz, and mode 3 covers from 3.6 to 6 GHz. There is about 380 MHz overlap between modes 2 and 3. However, there is an unfortunate 70 MHz gap between modes 1 and 2, and a few small gaps throughout the bands. It will affect quality factor of tank and also phase noise in circuit. For removing this deficiency form circuit a continuous tunable technique is proposed [2].

Sun *et al.* presents a dual-path PLL using a hybrid VCO to perform digital based frequency acquisition and analog based bandwidth control. With the mixed-mode dual-path control, the proposed PLL significantly alleviates noise coupling and area problems in the coarse-tuning path while minimizing open-loop gain variation in the fine-tuning path. In the hybrid VCO design, the nonlinearity issue of the capacitor array is addressed and a 1-bit quantizer delta sigma modulator is used to mitigate the problem. A 2 GHz PLL implemented in 0.18 m CMOS exhibits less than ± 3.5% bandwidth variation and less than 2 dB in-band noise variations over entire tuning range under nominal condition at room temperature. It also shows that more than 30 dB spur reduction is achieved with the bi-level second-order single-loop delta sigma modulator when the worst-case spur performance is compared with a second-order MASH modulator [6]. It was a mixed-mode dual-path PLL with a hybrid VCO is presented to achieve both a linear bandwidth

control and a low noise dual-path control over PVT variations over 2GHz at 0.18μm technology.

Chang *et al.* present a two-stage low-noise amplifier and a bottom-series coupled quadrature voltage-controlled oscillator (QVCO) using a 65-nm CMOS, it will improve tuning frequency up to 25 GHz with low phase noise. Here parasitic capacitance and the effective substrate resistance can be reduced. Moreover, the 3-dB cutoff frequency can be extended due to the reduction of the Miller effect. The bandwidth of the dual gate LNA is investigated to compare with the conventional cascade configuration. Besides, the operation principle of the quadrature signal generation using the dual-gate device is also presented for the QVCO design. The two-stage dual-gate LNA demonstrates a flat 3-dB bandwidth of 7.3 GHz from 19.4 to 26.7 GHz and a maximum gain of 18.9 dB. At 24 GHz, the measured minimum noise figure is 4.7 dB, and the measured output third-order intercept point is 11dBm. The dual-gate QVCO exhibits an oscillation frequency of up to 25.3 GHz, a phase noise of -109dBc/Hz at 1-MHz offset frequency, an amplitude error of 0.16 dB, and a phase error of 0.8°. The proposed dual-gate CMOS device is very suitable for the linear and nonlinear circuit designs above 20 GHz, especially for millimeter-wave applications due to its high speed and compact area. From above 25 GHz dual gate QVCO fail and produce high noise in circuit [15].

You Lu *et al.* present a 60 GHz, 16% tuning range VCO, and a 40 GHz, 18 bits, 14% tuning range DCO incorporating variable inductor (VID) techniques. Variable inductor consists of a transformer and a variable resistor. It is tunable by adjusting its resistor. By employing the proposed frequency tuning scheme, wide-tuning range as well as multi-band operation are achieved without sacrificing their operating frequencies. VCO and DCO are both fabricated in 90 nm CMOS technology. The tuning range of VCO is from 52.2 GHz to 61.3 GHz. The measured phase noise from a 61.3-GHz carrier is about -118.75dBc/Hz at 10-MHz offset, and the output power is -6.6dBm. It dissipates 8.7mW from a 0.7-V supply. On the other hand, the DCO is capable of covering frequency range from 37.6 GHz to 43.4 GHz. The measured phase noise from a 43 GHz carrier is about -109dBc/Hz at 10-MHz offset, and the output power is 11dBm. The DCO core dissipates 19mW from a 1.2-V supply. This VCO is based on magnetic tuning scheme rather than varactor tuning. It is capable of operating under a supply voltage as low as 0.7V, which is suitable for nanometer CMOS technology. Here Novel variable inductors for VCO and DCO are proposed. By using the magnetic frequency tuning scheme, both VCO and DCO are capable of operating at MMW frequency band while manifesting wider tuning range than those VCOs with varactors for frequency tuning [18]. As operating frequency will increase than their tuning range (%) will also decrease and difficult to maintain their low phase noise and low power consumption.

Wang *et al.* suggested a circuit topology suitable for a low-phase-noise wide-tuning-range push-push voltage-controlled oscillator (VCO) over 70 GHz. In this circuit topology varactors are connected between drain and source terminations of the cross coupled pair, the tuning range is

effectively increased and the phase noise is improved Moreover, a small capacitor is inserted between the VCO core and testing buffer to reduce loading effects on the VCO core. Furthermore, the enhanced second-harmonic output signal is extracted at middle of the varactors, leading to the elimination of RF choke at VCO's second-harmonic output port and a reduced chip size. This VCO is fabricated in 0.18-μm CMOS exhibits a measured 6.35% tuning range. Operating at a supply voltage of 1.2 V, the VCO core consumes 7.5-mW dc power, and the measured phase noise is −75dBc/Hz and −91.5dBc/Hz at 100-kHz and 1-MHz offsets from the 77.8-GHz carrier, respectively [12]. To predict the performance of fabricated VCO, the parasitic extraction of the layout has been performed by using full-wave electronic-magnetic (EM) simulation tools, Sonnet (Sonnet Software Inc., North Syracuse, NY) and HFSS (Ansys Inc., Canonsburg, PA). It is compared with previously published silicon-based VCOs over 70 GHz, this work can simultaneously achieve low phase noise, wide tuning range, and low dc power consumption, leading to a superior figure of merit (FOM), and better figure of merit considering the tuning range (FOM$_T$). In addition, this fully integrated VCO also demonstrates the highest operation frequency among previously published 0.18-μm CMOS VCOs. Today nanometer scale is replacing micrometer and CMOS is modified in SOI CMOS.

Sadhu *et al.* describes a new approach to low-phase noise LC VCO design based on Trans conductance linearization of the active devices. A 25 GHz VCO based on this linearization approach is integrated in a dual-path PLL and achieves superior performance compared to the state of the art. The design is implemented in 32 nm SOI CMOS technology and achieves a phase noise of -130dBc/Hz at a 10 MHz offset from a 22 GHz carrier. Additionally, a new layout approach for switched capacitor arrays that enables a wide tuning range of 23%. More than 1500 measurements of the PLL across PVT variations were taken, further validating the proposed design. Phase noise variation across supply voltages of 0.7–1.5 V is 2 dB and across 60° temperature variation is 3 dB. At the 25 GHz center frequency, the VCO FOM$_T$ is 188dBc/Hz. additionally, a digitally assisted autonomic biasing technique is implemented in the PLL to provide a phase noise and power optimized VCO bias across frequency and process. For the targeted 60-GHz application, a large frequency tuning range (FTR) is a critical requirement and switched capacitors on the drain and tank are utilized to manipulate the feedback ratio and extend linearization (and low phase-noise performance) over a large tuning range. The VCO frequency is less sensitive to capacitance variation on the drain node. As a result, the fine tuning capacitors and varactors are placed across the drain nodes for fine frequency control. For optimal phase noise, a small inductor is utilized. Consequently, the capacitor array and the inductor occupy comparable areas especially that associated with connecting the capacitor array, significantly impacts VCO performance. To mitigate this problem in the LiT VCO interconnect parasitic are minimized using a reduced-inductance layout technique [3] proposed by B. Sadhu in May 2013.

IV. CONCLUSION

Various design analysis used for implementation of PLL frequency synthesizer, has presented in this paper. For low phase noise, low power consumption, small chip area, wide tunning range and independent from PVT variation in nanometre CMOS/ SOI CMOS Technology has effectively improved their performance by using um or nm VLSI Technology. At higher frequency nm process (32-nm SOI CMOS) used to maintain tuning range as yet generated frequency range increases above from 60GHz their tuning range (%) would decrease. I have tried to focus on different approach taken by different research worker and their summarise prospect has presented here.

REFERENCES

[1] Young Lee, S. J. Yun, and Sang G Lee, "A Low-Parasitic and Common Centroid Cross Coupled CMOS Transistor Structure for High-Frequency VCO Design," *IEEE Electron Device Letters*, vol. 30, no. 5, May 2009, pp. 532 – 534.

[2] Zahra Safarian, and Hossein Hashemi, "Wideband Multi-Mode CMOS VCO Design Using Coupled Inductors," *IEEE Transactions on Circuits and Systems*, vol. 56, no. 8, August 2009, pp. 1830 – 1843.

[3] B. Sadhu, A. S. Natarajan, and R. Harjani, "A Linearized, Low-Phase-Noise VCO- Based 25 GHz PLL with Autonomic Biasing," *IEEE Journal of Solid- State Circuits*, vol. 48, no. 5, May 2013, pp. 1138 – 1150.

[4] M. M. Elsayed, M. Abdul-Latif, and Edgar Sanchez-Sinencio, "A Spur-Frequency- Boosting PLL With a -74 dBc Reference-Spur Suppression in 90 nm Digi- tal CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, September 2013, pp. 2104 – 2117.

[5] I. T. Lee, Y. T. Tsai, and S. I. Liu, "A Wide-Range PLL Using Self-Healing Prescaler/VCO in 65-nm CMOS," *IEEE Transaction on Very Large Scale Integration (Vlsi) System*, vol. 21, no. 2, February 2013, pp. 250 – 258.

[6] Y. Sun, J. Qiao, and X. Yu, "A Continuously Tuneable Hybrid LC-VCO PLL with Mixed-Mode Dual-Path Control and Bi-level Delta – Sigma Modulated Coarse Tuning," *IEEE Transaction on Circuits and System*, vol. 58, no. 9, September 2011, pp. 2149 – 2158.

[7] Ryan Lee Bunch, Sanjay Raman, "Large-Signal Analysis of MOS Varactors in CMOS -Gm LC VCO," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 8, August 2003, pp. 1325 – 1332.

[8] Paolo Maffezzoni, Salvatore Levantino, "Analysis of VCO Phase Noise in Charge-Pump Phase-Locked Loops," *IEEE Transactions on Circuits and Systems*, vol. 59, no. 10, October 2012, pp. 2165 – 2175.

[9] Karim M. Hussein, E. Hegazi, "An All-Analog Method to Enhance Amplitude Stability in Pierce Crystal Oscillators," *IEEE Transactions on Circuits and Systems*, vol. 59, no. 3, March 2012, pp. 463 – 470.

[10] Yao H. Kao, Meng T. Hsu, "Theoretical Analysis of Low Phase Noise Design of CMOS VCO," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 1, January 2005, pp. 33 – 35.

[11] S. Golestan, Mohammad Monfared, Francisco D. Freijedo, "Advantages and Challenges of a Type-3 PLL," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, November 2013, pp. 4985 – 4997.

[12] To-Po Wang , "A Fully Integrated W-Band Push-Push CMOS VCO With Low Phase Noise and Wide Tuning Range," *IEEE Transactions on Ultrasonic, Ferroelectrics, and Frequency Control*, vol. 58, no. 7, July 2011, pp. 1307 – 1319.

[13] B. Floyd, "A 16–18.8-GHz sub-integer-N frequency synthesizer for 60-GHz transceivers," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, May 2008, pp. 1076–1086.

[14] Guansheng Li, Y. Tang, E. Afshari, "A Low-Phase-Noise Wide-Tuning-Range Oscillator Based on Resonant Mode Switching," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 6, June 2012, pp. 1295 – 267.

[15] H. Y. Chang, C. H. Lin, "65-nm CMOS Dual-Gate Device for Ka-Band Broadband Low-Noise Amplifier and High-Accuracy Quadrature Voltage-Controlled Oscillator," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 6, June 2013, pp. 2402 – 2413.

[16] S. Pellerano, "A 39.1 to 41.6 GHz fractional-N frequency synthesizer in 90 nm CMOS," *in Proc. IEEE Int. Solid-State Circuits*, February 2008, pp. 484 – 630.

[17] D. Murphy *et al.*, "A low phase noise wideband and compact CMOS PLL for use in a heterodyne transceiver," *IEEE J. Solid-State Circuits,* vol. 46, no. 7, July 2011, pp. 1606–1617.

[18] Tai Y. Lu, Chi Y. Yu, Wei Z. Chen , "Wide Tunning Range 60 GHz VCO and 40 GHz DCO Using Single Variable Inductor," *IEEE Transactions on Circuits and Systems*, vol. 60, no. 2, February 2013, pp. 257 – 267.

[19] W. Wu, R. B. Staszewski, and J. R. Long, "A 56.4-to-63.4 GHz Multi-Rate All-Digital Fractional-N PLL for FMCW Radar Applications in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 5, May 2014. (Accepted)

[20] Neha S. Digrase, and D. S. Chaudhari, "An Overview: RF Design of Fast Locking Digital Phase Locked Loop," *International Journal of Advanced Research in Computer Science and Software Engineering*, vol. 3, no. 3, March 2013, pp. 389 – 392.